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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

FINGHAI HAO ET AL.

Serial No. 10/670,434 (TI-35470)

Filed September 23, 2003

For: REDUCTION OF CHANNEL HOT CARRIER EFFECTS IN TRANSISTOR DEVICES

Art Unit 2823

Examiner Khiem D. Nguyen

Customer No. 23494

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Jay M. Cantor, Reg. No. 19,906

Sir:

## BRIEF ON APPEAL

## REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

## RELATED APPEALS AND INTERFERENCES

There is an appeal in divisional application Serial No. 11/135,544.

## STATUS OF CLAIMS

This is an appeal of claims 1 to 22, all of the rejected claims. The invention of cancelled claims 22 to 27 is the subject of a divisional application referenced above. Please charge any costs to Deposit Account No. 20-0668.

## STATUS OF AMENDMENTS

An amendment was not filed after a second final rejection.

## SUMMARY OF CLAIMED SUBJECT MATTER

According to claims 1 to 12 the claimed invention relates to a method for fabricating a transistor structure which includes the steps of providing a substrate having a surface and a channel region (26, 100) and forming a lightly doped drain (LDD) region (108, 20) in the substrate contiguous to the channel region (portion of substrate beneath the gate) and the surface. A first dopant (114) having a lower dopant concentration than that of the LDD region is implanted into the lightly doped drain (LDD) region to a depth less than the LDD junction depth (112) and a second dopant (122) is implanted into the substrate *beyond* the LDD junction depth to form a source/drain region (120), the implantation of the second dopant of sufficient dopant concentration to overpower a portion of the LDD remote from the channel and a substantial portion of the first dopant to define a floating region of the first dopant completely within the LDD region (124), the source/drain region and the surface and remote from the channel region with reduced dopant concentration relative to the dopant concentration of the LDD region (page 5, line 15ff). The floating region can further comprise a floating ring substantially self-alinged with an edge of a gate (106) of the transistor structure (page 9, line 30ff). The LDD region can be formed by implanting a dose of an LDD dopant that is greater than a dose of the first dopant.

The dose of the first dopant can be being about twenty-percent or less of the dose of the LDD dopant. At least one of the implantation of the first dopant and the implantation of the LDD dopant can employ tilted angle implants to enhance an amount of overlap between a gate structure of the transistor structure and the LDD region. The dose of the second dopant can be greater than the dose of the LDD dopant. The LDD dopant can further comprise implanting a dose of an n-type dopant in a range from about $1e^{13}$ $cm^2$ to about $5e^{14}$ $cm^2$, and the implantation of the first dopant further comprising implanting a dose in a range from about $1e^{12}$ $cm^2$ to about $5e^{14}$ $cm^2$ of a p-type dopant.. The transistor structure can be a complimentary metal oxide semiconductor (CMOS) structure that includes a gate having a side edge portion, the floating region being substantially aligned with the side edge portion of the gate and the CMOS structure can be an n-channel CMOS structure, the first dopant forming a shallow region in the LDD region that comprises a p-type dopant wherein the first dopant can comprise boron, and the floating region can further comprise a boron floating ring substantially aligned with side edge portion of the gate. The CMOS structure can be a p-channel CMOS structure, the first dopant defining a shallow region that comprises an n-type dopant (page 6, line 4ff). The gate structure can be formed above the substrate, the LDD region and the source/drain region in the substrate generally around the gate structure, the gate structure overlapping at least a substantial portion of the LDD region and the floating ring being substantially aligned with an edge of the gate structure.

According to claims 13 to 22, the claimed invention relates to a method for fabricating a CMOS transistor device, comprising the steps of providing a substrate having a surface and a channel region (26, 100) and forming a gate structure (106) on the ~~a~~ substrate, the gate structure having a side edge. Then forming a lightly doped drain (LDD) region (108) in the substrate

laterally of the channel region and extending to the surface and beneath the gate structure and then forming a shallow region in the LDD region having a lower dopant concentration than that of the LDD region that extends to the surface and into the substrate to a depth that is less than an LDD junction depth and spaced from said channel region (112). Then a source/drain region is formed (120), formation of the source/drain region resulting in forming a floating structure from the shallow region that is located completely within the LDD region, the source/drain region and the surface and generally aligned with the side edge of the gate structure (124), the floating structure having reduced dopant concentration relative to the doping concentration of the LDD region. The LDD region can be formed with a dose of a dopant that is greater than a dose of a dopant utilized to form the shallow region. The dose of the dopant that is utilized to form the shallow region can be at least approximately twenty-percent less than the dose of the dopant that is utilized to form the LDD region. The LDD region can further comprise implanting a dose of an n-type dopant in a range from about $1e^{13}$ $cm^2$ to about $5e^{15}$ $cm^2$, and the formation of the shallow region can further comprise implanting a dose in a range from about $1e^{12}$ $cm^2$ to about $1e^{14}$ $cm^2$ of a p-type dopant. At least one of the implantation of the formation of the LDD region and the formation of the shallow region can further comprise employing tilted angle implants to increase an amount of overlap beneath the gate structure. The formation of the source/drain region can be implemented with a dose of a dopant that is greater than a dose of a dopant utilized to form each of the LDD region and the shallow region. The CMOS structure can be an n-channel CMOS structure, the shallow region comprising a p-type dopant. The shallow region can comprise boron, the floating structure comprising a boron floating ring substantially aligned with the side edge of the gate structure. The CMOS structure can be a p-channel CMOS structure, the shallow region comprising an n-type dopant.

## GROUNDS OF REJECTION

Claims 1 to 22 were rejected under 35 U.S.C.102(b) as being anticipated by Nowak et al. (U.S. 6,528,846).

## ARGUMENT

Claims 1 to 22 were rejected under 35 U.S.C. 102(b) as being anticipated by Nowak et al. (U.S. 6,528,846). The rejection is without merit.

It is elementary that, for a rejection to be proper under 35 U.S.C. 102(b), it is necessary that each and every feature claimed be found in a single reference or be inherent therein. This is not the case herein as will be demonstrated.

With reference to claim 1, this claim requires, among other steps, the step of implanting a second dopant into the substrate *beyond* the LDD junction depth to form a source/drain region, the implantation of the second dopant of sufficient dopant concentration to overpower a portion of the LDD remote from said channel and a substantial portion of the first dopant to define a floating region of the first dopant completely within the LDD region, the source/drain region and said surface and remote from said channel region with reduced dopant concentration relative to the dopant concentration of the LDD region. No such step is taught or suggested by Nowak et al. Nowhere in Nowak et al. is the source/drain region disposed in the substrate *beyond* the LDD region.

Claims 2 to 12 depend from claim 1 and therefore define patentably over Nowak et al. for at least the reason presented above with reference to claim 1.

In addition, claim 2 requires that the floating region further comprise a floating ring substantially self-aligned with an edge of a gate of the transistor structure. The element 21 of

Nowak et al. is not shown to be self-aligned with the gate structure but rather with the oxide layer 17 on the sidewall of the gate structure.

Claim 5 further limits claim 3 by requiring that at least one of the implantation of the first dopant and the implantation of the LDD dopant employ tilted angle implants to enhance an amount of overlap between a gate structure of the transistor structure and the LDD region. No such feature is taught or suggested by Nowak et al. either alone or in the combination as claimed. It is elementary that an allegation that the feature is known in the prior art is not a basis for a rejection under section 102.

Claim 6 further limits claim 3 by requiring that the dose of the second dopant be greater than the dose of the LDD dopant. The examiner has not shown where in the specification of Nowak et al. this is shown. A referral to almost the entire specification is not such a showing.

Claim 8 further limits claim 1 by requiring that the transistor structure be a complimentary metal oxide semiconductor (CMOS) structure that includes a gate having a side edge portion, the floating region being substantially aligned with the side edge portion of the gate. No such feature is taught or suggested by Nowak et al. The region 21 of Nowak et al. is not shown substantially aligned with the side edge portion of the gate, but rather with the oxide sidewall on the gate.

Claim 10 further limits claim 9 by requiring that the first dopant comprise boron, and the floating region further comprises a boron floating ring substantially aligned with side edge portion of the gate. No such feature is taught by Nowak et al.

Claim 12 further limits claim 1 by requiring forming a gate structure above the substrate, the LDD region and the source/drain region being formed in the substrate generally around the gate structure, the gate structure overlapping at least a substantial portion of the LDD region and

the floating ring being substantially aligned with an edge of the gate structure. No such feature is taught or suggested by Nowak et al. in view of the location of the floating ring as claimed as discussed above.

Claim 13 requires, among other features, forming a source/drain region, formation of the source/drain region resulting in forming a floating structure from the shallow region that is located completely within the LDD region, the source/drain region and the surface and generally aligned with the side edge of the gate structure, the floating structure having reduced dopant concentration relative to the doping concentration of the LDD region. As discussed above, the structure 21 of Nowak et al. is not aligned with the gate structure but rather with the oxide sidewall on the gate structure.

Claim 14 to 22 depend from claim 13 and therefore define patentably over Nowak et al. for at least the reason presented above with reference to claim 13.

Claim 17 further limits claim 13 by requiring that at least one of the implantation of the formation of the LDD region and the formation of the shallow region further comprise employing tilted angle implants to increase an amount of overlap beneath the gate structure. The argument presented above with reference to claim 5 is applicable and incorporated by reference.

Claim 20 further limits claim 19 by requiring that the shallow region comprise boron, the floating structure comprising a boron floating ring substantially aligned with the side edge of the gate structure. The argument presented above with reference to claim 10 applies and is incorporated by reference.

## CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(301) 424-0355
(972) 917-5293

# CLAIMS APPENDIX

The claims on appeal read as follows:

1. A method for fabricating a transistor structure, comprising the steps of:

providing a substrate having a surface and a channel region;

forming a lightly doped drain (LDD) region in said substrate contiguous to said channel region and said surface;

implanting a first dopant having a lower dopant concentration than that of said LDD region into said lightly doped drain (LDD) region to a depth less than the LDD junction depth; and

implanting a second dopant into said substrate beyond the LDD junction depth to form a source/drain region, the implantation of the second dopant of sufficient dopant concentration to overpower a portion of the LDD remote from said channel and a substantial portion of the first dopant to define a floating region of the first dopant completely within the LDD region, the source/drain region and said surface and remote from said channel region with reduced dopant concentration relative to the dopant concentration of the LDD region.

2. The method of claim 1, the floating region further comprising a floating ring substantially self-aligned with an edge of a gate of the transistor structure.

3. The method of claim1, further comprising forming the LDD region by implanting a dose of an LDD dopant that is greater than a dose of the first dopant.

4. The method of claim 1, the dose of the first dopant being about twenty-percent or less of the dose of the LDD dopant.

5. The method of claim 3, at least one of the implantation of the first dopant and the implantation of the LDD dopant employing tilted angle implants to enhance an amount of overlap between a gate structure of the transistor structure and the LDD region.

6. The method of claim 3, the dose of the second dopant being greater than the dose of the LDD dopant.

7. The method of claim 3, the implantation of the LDD dopant further comprising implanting a dose of an n-type dopant in a range from about $1e^{13}$ $cm^2$ to about $5e^{14}$ $cm^2$, and the implantation of the first dopant further comprising implanting a dose in a range from about $1e^{12}$ $cm^2$ to about $5e^{14}$ $cm^2$ of a p-type dopant..

8. The method of claim 1, the transistor structure is a complimentary metal oxide semiconductor (CMOS) structure that includes a gate having a side edge portion, the floating region being substantially aligned with the side edge portion of the gate.

9. The method of claim 8, the CMOS structure is an n-channel CMOS structure, the first dopant forming a shallow region in the LDD region that comprises a p-type dopant.

10. The method of claim 9, the first dopant comprises boron, and the floating region further comprises a boron floating ring substantially aligned with side edge portion of the gate.

11. The method of claim 8, the CMOS structure is a p-channel CMOS structure, the first dopant defining a shallow region that comprises an n-type dopant.

12. The method of claim 1, further comprising:

forming a gate structure above the substrate, the LDD region and the source/drain region being formed in the substrate generally around the gate structure, the gate structure overlapping at least a substantial portion of the LDD region and the floating ring being substantially aligned with an edge of the gate structure.

13. A method for fabricating a CMOS transistor device, comprising the steps of:

providing a substrate having a surface and a channel region and forming a gate structure on said ~~a~~ substrate, the gate structure having a side edge;

forming a lightly doped drain (LDD) region in the substrate laterally of said channel region and extending to said surface and beneath said gate structure;

then forming a shallow region in the LDD region having a lower dopant concentration than that of the LDD region that extends to said surface and into the substrate to a depth that is less than an LDD junction depth and spaced from said channel region; and

then forming a source/drain region, formation of the source/drain region resulting in forming a floating structure from the shallow region that is located completely within the LDD region, the source/drain region and said surface and generally aligned with the side edge of the gate structure, the floating structure having reduced dopant concentration relative to the doping concentration of the LDD region.

14. The method of claim 13, the LDD region being formed with a dose of a dopant that is greater than a dose of a dopant utilized to form the shallow region.

15. The method of claim 14, the dose of the dopant that is utilized to form the shallow region is at least approximately twenty-percent less than the dose of the dopant that is utilized to form the LDD region.

16. The method of claim 13, the formation of the LDD region further comprising implanting a dose of an n-type dopant in a range from about $1e^{13}$ $cm^2$ to about $5e^{15}$ $cm^2$, and the formation of the shallow region further comprising implanting a dose in a range from about $1e^{12}$ $cm^2$ to about $1e^{14}$ $cm^2$ of a p-type dopant.

17. The method of claim 13, at least one of the implantation of the formation of the LDD region and the formation of the shallow region further comprising employing tilted angle implants to increase an amount of overlap beneath the gate structure.

18. The method of claim 13, the formation of the source/drain region being implemented with a dose of a dopant that is greater than a dose of a dopant utilized to form each of the LDD region and the shallow region.

19. The method of claim 13, the CMOS structure is an n-channel CMOS structure, the shallow region comprising a p-type dopant.

20. The method of claim 19, the shallow region comprising boron, the floating structure comprising a boron floating ring substantially aligned with the side edge of the gate structure.

21. The method of claim 13, the CMOS structure is a p-channel CMOS structure, the shallow region comprising an n-type dopant.

22. A transistor structure formed according to the method of claim 13.

## EVIDENCE APPENDIX

Not applicable

## RELATED PROCEEDINGS APPENDIX

See RELATED APPEALS AND INTERFERENCES on page 1 supra.